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Claims

[c1] 1.A dual-mode Universal-Serial-Bus (USB) switch comprising:

a USB upstream interface to a host USB bus for connecting to a host;

a plurality of USB downstream interfaces that connect to USB bus segments for connecting to a plurality of memory blocks;

a virtual USB bridge for connecting the USB upstream interface to the plurality of USB downstream interfaces; and

a transaction manager, coupled to control the virtual USB bridge to act as a USB hub by passing USB packets from the host to the plurality of memory blocks through the virtual USB bridge when operating in a hub mode, but for acting as a single USB endpoint to the host when operating in a single-endpoint mode;

wherein the transaction manager passes data between the host and the memory blocks but intercepts and modifies packets from the host to generates secondary USB packets over the USB bus segments to the memory blocks when operating in the single-endpoint mode;

wherein the memory blocks and the USB bus segments

are hidden from the host by the transaction manager when operating in the single-endpoint mode, but visible as USB endpoints to the host when operating in hub mode,

whereby the dual-mode USB switch operates in modes having multiple endpoints or a single endpoint for multiple downstream memory blocks.

[c2] 2.The dual-mode USB switch of claim 1 further comprising:

mode logic, coupled to the transaction manager, for determining when to set the transaction manager in the hub mode and when to set the transaction manager in the single-endpoint mode.

[c3] 3.The dual-mode USB switch of claim 2 wherein the mode logic is coupled to sense a voltage of a mode pin that is driven externally to a predetermined voltage to cause the transaction manager to operate in the single-endpoint mode.

[c4] 4.The dual-mode USB switch of claim 1 further comprising:

a virtual storage processor, coupled to the transaction manager, for translating a logical address from the host to a physical address for accessing requested data from the memory blocks.

[c5] 5.The dual-mode USB switch of claim 4 wherein the virtual storage processor further translates the physical address to a plurality of addresses of multiple memory blocks that contain the requested data when data is stored in stripes across multiple memory segments.

[c6] 6.The dual-mode USB switch of claim 4 wherein the transaction manager determines a plurality of memory capacities of the memory blocks presently connected to the plurality of USB downstream interfaces by the USB bus segments;
wherein the transaction manager reports a sum of the plurality of memory capacities to the host as a memory capacity of a single virtual USB memory device when operating in the single-endpoint mode,
whereby memory capacities are aggregated.

[c7] 7.The dual-mode USB switch of claim 6 wherein the virtual storage processor stores attributes of the memory blocks but the transaction manager reports a composite attribute to the host when queried by the host for device attributes.

[c8] 8.The dual-mode USB switch of claim 7 wherein the memory blocks appear as a single USB memory device to the host because the transaction manager acts as a sin-

gle USB endpoint having a single-endpoint USB device address on the host USB bus;
wherein the transaction manager replaces USB device addresses of the memory blocks with the single-endpoint USB device address when converting secondary packets from the USB bus segments to packets to the host.

[c9] 9.The dual-mode USB switch of claim 1 wherein the transaction manager re-orders secondary packets to the memory blocks on the USB bus segments relative to a packet order of corresponding packets on the host USB bus to initiate overlapping accesses of two of the memory blocks.

[c10] 10.The dual-mode USB switch of claim 9 wherein a second token packet with a command to access data in a second of the memory blocks is re-ordered to be sent over the USB bus segments before a first handshake packet that completes a first transaction.

[c11] 11.The dual-mode USB switch of claim 9 wherein a first transaction on the host USB bus comprises a first token packet with a command to access memory, a first data packet containing data accessed, and a first handshake packet ending the first transaction;
wherein a second transaction on the host USB bus comprises a second token packet with a command to access

memory, a second data packet containing data accessed, and a second handshake packet ending the second transaction;

wherein the packet order on the host USB bus is the first token packet, the first data packet, the first handshake packet, the second token packet, the second data packet, and the second handshake packet, respectively;

wherein the transaction manager re-orders the second token packet to before the first data packet so that a packet order on the USB bus segments to the memory blocks is a sequence of secondary packets that correspond to the first token packet, the second token packet, the first data packet, the first handshake packet, the second data packet, and the second handshake packet, respectively,

whereby the second token packet is re-ordered on the USB bus segments to overlap the second transaction with the first transaction.

[c12] 12.The dual-mode USB switch of claim 11 wherein packets are re-ordered when data requested by the first and second transactions are to different and non-overlapping memory locations, but packets are not re-ordered when data requested by the first and second transactions are overlapping memory locations.

[c13] 13.The dual-mode USB switch of claim 9 wherein the virtual USB bridge comprises:
an internal bus for transferring USB packets;
an upstream virtual USB bridge for connecting the USB upstream interface to the internal bus;
a plurality of downstream virtual USB bridges for connecting the plurality of USB downstream interfaces to the internal bus.

[c14] 14.The dual-mode USB switch of claim 13 wherein the memory blocks comprise a plurality of USB flash storage blocks containing flash memory.

[c15] 15.A packet re-ordering USB switch comprising:
an upstream interface to a host USB bus that connects to a host;
a transaction manager, coupled to the upstream interface, for sending and receiving USB packets to and from the host, the USB packets arranged in transactions having a token packet to initiate a transaction, a data packet when data is transferred, and a handshake packet to end the transaction;
a first downstream interface to a first downstream bus to a first flash storage block;
a second downstream interface to a second downstream bus to a second flash storage block;
a third downstream interface to a third downstream bus

to a third flash storage block; and

an internal bus between the transaction manager, the first downstream interface, the second downstream interface, and the third downstream interface;

wherein the transaction manager re-orders a second token packet from a second transaction to be sent to the first, second, or third flash storage block before the handshake packet of a first transaction that immediately precedes the second transaction when overlapping transactions,

whereby the second token packet is re-ordered to overlap transactions to the first, second, and third flash storage blocks.

[c16] 16.The packet re-ordering USB switch of claim 15 further comprising:

a virtual storage processor, coupled to the transaction manager, for reading and storing attributes of the first, second, and third flash storage block, and for generating addresses to the first, second, and third flash storage block in response to data requests from the host;

wherein the transaction manager reports as a single USB endpoint to the host, but transfers data between the host and the first, second, and third flash storage block, whereby a single USB endpoint is reported to the host for the first, second, and third flash storage block by the

transaction manager.

[c17] 17.The packet re-ordering USB switch of claim 16 wherein the virtual storage processor signals to the transaction manager to overlap a first and a second transaction when the first and second transaction each access a different one of the first, second, and third flash storage blocks.

[c18] 18.An aggregating serial-bus hub/switch comprising:
upstream interface means for connecting to a host bus to a host;
a plurality of downstream interface means, connected to bus segments, for serially interfacing to a plurality of memory blocks;
virtual bridge means for connecting the upstream interface means to the plurality of downstream interface means; and
transaction manager means for controlling the virtual bridge means to act as a hub by passing packets from the host to the plurality of memory blocks through the virtual bridge means when operating in a hub mode, but for acting as a single endpoint to the host when operating in a single-endpoint mode;
wherein the transaction manager means passes data between the host and the memory blocks but intercepts and modifies packets from the host to generates sec-

ondary packets over the bus segments to the memory blocks when operating in the single-endpoint mode;
wherein the transaction manager means includes means for re-ordering the secondary packets to the memory blocks on the bus segments relative to a packet order of corresponding packets on the host bus to initiate overlapping accesses of two of the memory blocks;
wherein the memory blocks and the bus segments are hidden from the host by the transaction manager means when operating in the single-endpoint mode, but visible as endpoints to the host when operating in hub mode, whereby the dual-mode switch operates in modes having multiple endpoints or a single endpoint for multiple downstream memory blocks.

[c19] 19.The aggregating serial-bus hub/switch of claim 18 further comprising:
virtual storage processor means, coupled to the transaction manager means, for translating a logical address from the host to a physical address for accessing requested data from the memory blocks.

[c20] 20.The aggregating serial-bus hub/switch of claim 19 wherein the host bus is a Universal-Serial-Bus (USB), a PCI Express bus, an ExpressCard bus, a Firewire IEEE 1394 bus, a serial ATA bus, or a serial attached small-computer system interface (SCSI) bus;

wherein the bus segments are each a USB, a PCI Express bus, a Firewire IEEE 1394 bus, a serial ATA bus, or a serial attached small-computer system interface (SCSI) bus.